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ESTUDIO DE CASO

Operación del convertidor dc/dc puente completo condesplazamiento de fase y conmutación a tensión cero: análisis y consideraciones de diseño

Operation of the phase-shifted zero-voltage-switching full-bridge dc/dc converter: analysis and design considerations

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Resumen

El convertidor DC/DC puente completo es tal vez una de las topologías más ampliamente adoptadas en aplicaciones de media y alta potencia debido a su capacidad de lograr la conmutación de sus interruptores bajo condiciones de tensión cero (Zero-Voltage-Switching ZVS) reduciendo así las pérdidas y mejorando el rendimiento general del convertidor. Este artículo presenta una revisión detallada del principio de funcionamiento y consideraciones de diseño del convertidor bajo condiciones de conmutación suave. De manera adicional se evalúan las características de desempeño a través de simulación.

Palabras claves: Conmutación Suave, Convertidores DC/DC, Electrónica de Potencia.

Abstract

The Phase-Shifted Full-Bridge DC/DC converter is a widely adopted topology in medium to high power applications due to its capability of achieving Zero-Voltage-Switching (ZVS) of the primary switches, reducing commutation losses and increasing the overall performance of the converter. This paper presents a detailed review of the operating principle and desing considerations for achieving ZVS in Phase-Shifted Full-Bridge DC/DC converters.Additionally, certain performance characteristics are evaluated through simulation.

Keywords: Soft-Switching, DC/DC Converters, Power Electronics.

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INTRODUCTION

Most modern medium and high-power converter applications in isolated topologiessuch as half or full bridge convertersuse power MOSFETs technologies. The Phase-Shifted Full-Bridge DC/DC converter is one of the most widely adopted soft-switched topology in high power applications (Capua, Shirsavar, Hallworth, Femia, & Member, 2015; Mweene, Wright, & Schlecht, 1989; Sabate, Vlatkovic, Ridley, Lee, & Cho, 1990).This converter features Zero-Voltage-Switching (ZVS), high operating frequency and high efficiency. Furthermore, the soft-switched operation of this topology, allows a reduction in the produced electromagnetic interference EMI (Emami, Nikpendar, Shafiei, & Motahari, 2011).The stray components such as the output capacitance of the power MOSFETs and the leakage inductance of the transformer are used advantageously to provide zero voltage turn-on of the switches (Gwan-Bon, Tae-Sung, Gun-Woo, & Myung-Joong, 2004). Althoughan increased leakage inductance can extend the load range for ZVS operation, it can also impact negatively the performance of the converter (Bodur & Bakan, 2004; Zhang, Xie, Wu, & Qian, 2004). ZVS operation of the converter can be achieved easily, improvingthe converter performance, however, in order to exploit the advantages of this topology it is important to take under special consideration the side effects of the ZVS operation and a proper design of the converter.

PRINCIPLE OF OPERATION

Traditionally a Full-bridge DC/DC converter, as the one presented in figure 1 (left), turns a diagonal pair of switches simultaneously. This reflects the input voltage across the primary of the transformer with an alternating polarity depending on the pair of diagonal switches simultaneously gated.

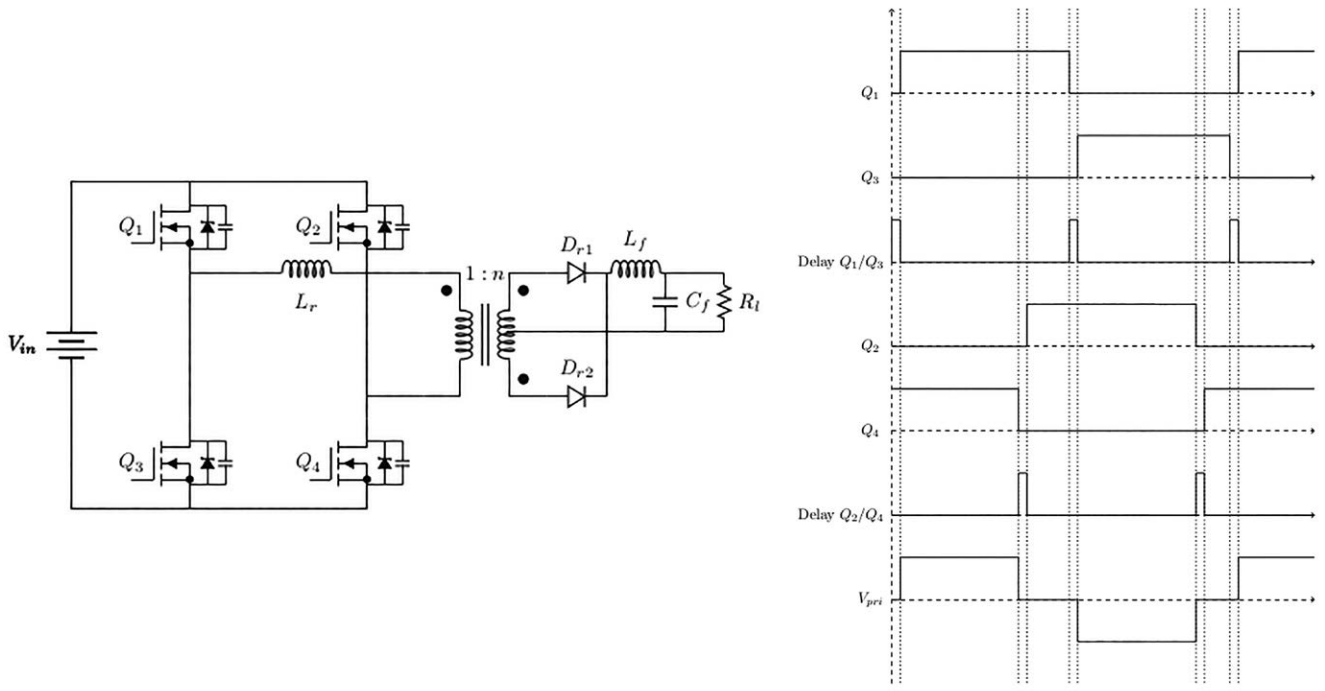

Figure 1. Conventional Full-Bridge DC/DC Converter (Left) Gating Signals on Phase-Shifted Control (Right)

Source: Own Creation

In contrast, the phase-shifted converter introduces a phase shift in the gating signals of the switches, this shift determinesthe operating duty cycle and also forces the primary currentto flow continuosly in the primary side of the converterduring the free-wheeling period.Figure 1 (right) depicts the gating signals and the required dead times between transitions to achieve ZVS operation in the full bridge converter while operating in continuos current mode.Let *Cm* be the output capacitance of one switch, *Cxfrmr* is the inter-winding capacitance of the transformer. At any given transition interval the energy stored in the leakage inductance must be enough to drive the combined capacitances of two switches and the transformer inter-winding capacitance, this combination will be referred as the resonant capacitance *Cres* and is given by the equation (1):

$$C_{res} = \left(\frac{8}{3}C_m + \frac{1}{2}C_{xfrmr}\right) \quad (1)$$

Cm is multiplied by an adjustment factor of $\frac{8}{3}$ to approximate the average output capacitance value of power MOSFETS due to its highly non linear operation. Moreover two capacitors are driven in the transition interval so the total capacitance is doubled.

The condition for ZVS operation is given by the equation (2):

$$E_l = \frac{1}{2}L_{res}I^2 \geq \frac{1}{2}C_{res}V_{in}^2 \quad (2)$$

Where *El* is the inductive energy stored in the resonant inductance *Lres*. *I* is the primary current at the time of the transition.

The bridge begins its operation with switches *Q*1 and *Q*4 on. The input voltage is reflected in the primary side of thetransformer with a positive polarity with respect to its dottedterminal. The primary current is increased positively to a peakvalue of Ipeak as shown in figure 2. The rectifier diode D_{r1} is forward-biased and therefore power is being transferred tothe load.To begin the transition between the bridge legs, switch *Q*4 is turned off instantly at t_0. The power transfer interval has just ended and the output inductor current is reflected to the primary and becomes the source of energy to displace the charge from the capacitors on the

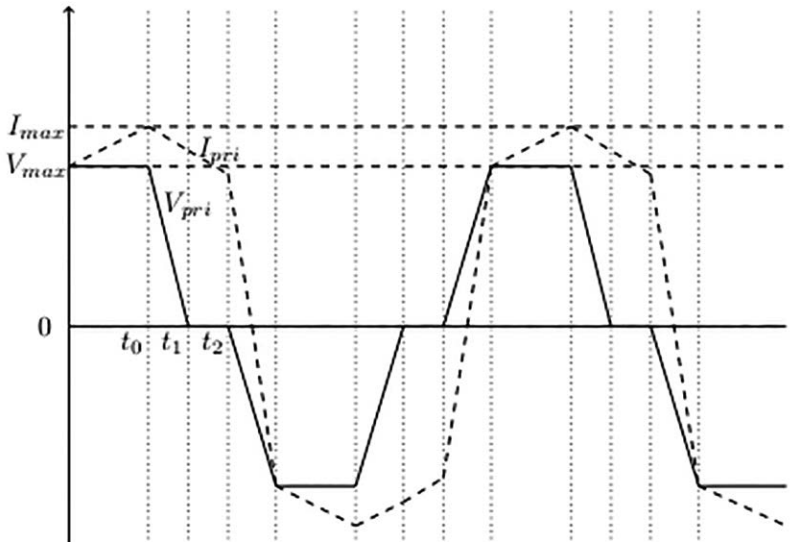

Figure 2. Primary Voltage And Current Waveforms

Source: Own Creation

right leg of the converter and fromthe inter-winding capacitance of the transformer also. Whilethe output capacitance of switch $Q2$ discharges, its body diodestarts conducting and places $Q2$ with virtually no drain to source voltage, facilitating lossless turn-on.

The mechanism by which ZVS is achieved in the rightleg transition is different from the one for the left leg.In theright leg case, the output inductor current is modelled as aconstant current source reflected to the primary that drivesthe output capacitance of the switches and transformer. The minimum required time for this transitions to happen is given by the equation (3):

$$t_{rl} = \frac{C_{res} V_{in}}{I_{peak}} \tag{3}$$

Once the transition is complete, the primary current startsfree-wheeling through $Q1$ and $D2$ This places the primaryside of the transformer across the upper voltage rail andforces its voltage to zero, switch $Q2$ now turns on and $Q1$ is now ready to be turned off. The primary current continues decreasing and only can change its direction until theprimary of the transformer has fully reversed its polarity. Switch $Q1$ switches off instantly at time $t2$ as depicted in figure 1, the current now continues to flow through its output capacitance chargingit and discharging the output capacitance of switch $Q3$. $Q3$ will turn-on with zero voltage only if a delay betweenthe turn-off of $Q1$ and the turn-on of $Q3$ is introduced. This delay is necessary for the resonant voltage produced by L_{res} and C_{res} to fully resonate at zero, the waveform of this voltage is depicted in figure 3. The periodof this waveform must be at least four times higher thanthe maximum transition time t_{lt} in order to achieve ZVS condition, this is:

$$t_{lt} = \frac{T_{res}}{4} \tag{4}$$

If the aforementioned condition is not met, ZVS condition is lost.

The angular frequency is given by the equation (5):

$$\omega = \sqrt{L_{res} C_{res}} = \frac{2\pi}{T_{res}} \tag{5}$$

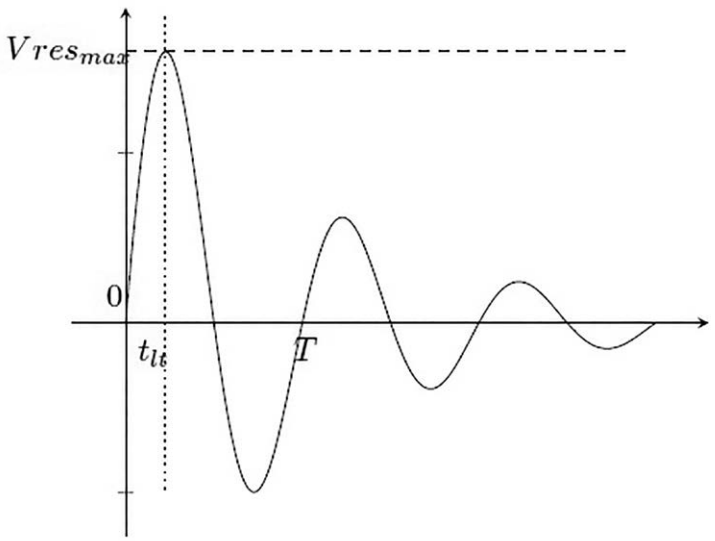

Figure 3. Waveform Of Voltage Produced By The Resonant Tank

Source: Own Creation

Finally, the required dead time for the left leg transition to achieve ZVS conditioncan be expressed in the equation (6):

$$t_{lt} = \frac{\pi}{2}\sqrt{L_{res}C_{res}} \quad (6)$$

DESIGN CONSIDERATIONS

The choice of the switching frequency of the converter must be made to meet the power density and application requirements, however special attention must be paid to the required dead times when operating at low-loador no load conditions to still achieve an efficient lossless ZVS operation. The selection of the primary resonant inductance must be made so that the energy requirements for low-load be accomplished andalso reduce the secondary duty cycle loss (Sabate et al., 1990). Let δ lT be the time it takes for the primary current to fully reverse its direction. If the primary current is the load current reflected to the primary side, then:

$$L_{res} = \frac{\delta 1T\, V_{in} N_p}{2\, I_{load} N_s} \quad (7)$$

Equation 7 allows to compute the value of L_{res} in terms of the duty cycle loss. It is desirable to reduce the capacitive energy in the circuit rather than increase the inductive energy.Selecting switches with low output capacitance is strongly advised, also the selection of the secondary rectifiers must be made to reduce the voltage ringing. A voltage ringing happens when the voltage in the transformer rises, the junction capacitance of the reverse biased rectifier rings with the leakage inductance of the transformer and can reach a peak value as high as three times the voltage applied to the secondary (Sabate et al., 1990). A clamping scheme proposed by Mweene (Mweene et al., 1989) clamps the maximum peak voltage of the ringing and returns part of the energy to the output filter.

Table 1. Design Parameteres of the Converter

Parameter	Value
Input Voltage (V)	170
Output Voltage (V)	30
Filter Inductor (uH)	1.15
Filter Capacitor (uF)	10
Load Resistance (Ω)	1.6
Switching Frequency (kHz)	500
Transfomer Total primary Resonant Inductance L_{res} (uH)	2
Secondary Inductance per Winding (uH)	0.5

Source: Own Creation

Table 2. Switching Devices Parameters

Parameter	Value
Output Capacitance Coss (pF)	1000pF @ Vgs=0, Vds=25, f=1Mhz
On Resistance RdsOn (mΩ)	0.27
Vds (V)	500
Ids (A)	21

Source: Own Creation

PERFORMANCE CHARACTERISTICS OF ZVS OPERATION

To verify the working principle of the ZVS converter exposed above,simulations were carried out using Orcad PSPICE. The design parameters are presented in table 1.

The switches used for simulation were IRF460N the characteristics of this switches are summarizedin table 2:

To compute the total resonant capacitance the output capacitance of the switches must be adjusted to accommodate the operating voltage level as follows:

$$C = C_{25}\sqrt{\frac{25\,V}{v}} \tag{8}$$

Where C_{25} is the output capacitance given in the device datasheet and measured by themanufacturer at standard test conditions (Vgs = 0 Vds = 25, f = 1Mhz). v is the operatingvoltage of the switch and Cm is the adjusted capacitance.The inter-winding capacitance of the transformer was neglected. Using the equation (8) the total capacitance per switch becomes:

$$C_m = 1000\,pF\sqrt{\frac{25\,V}{170\,V}} = 380\,pF \tag{9}$$

And the total resonant capacitance *Cres* is:

$$C_{res} = \frac{4}{3}C_m \approx 507\,pF \tag{10}$$

Using Equations (3) and (6), the required dead times for each leg transistions were computed and introduced in the switching scheme of the converter. Table 3 summarizes the instantaneous power dissipated by every switching device at turn on and turn off.

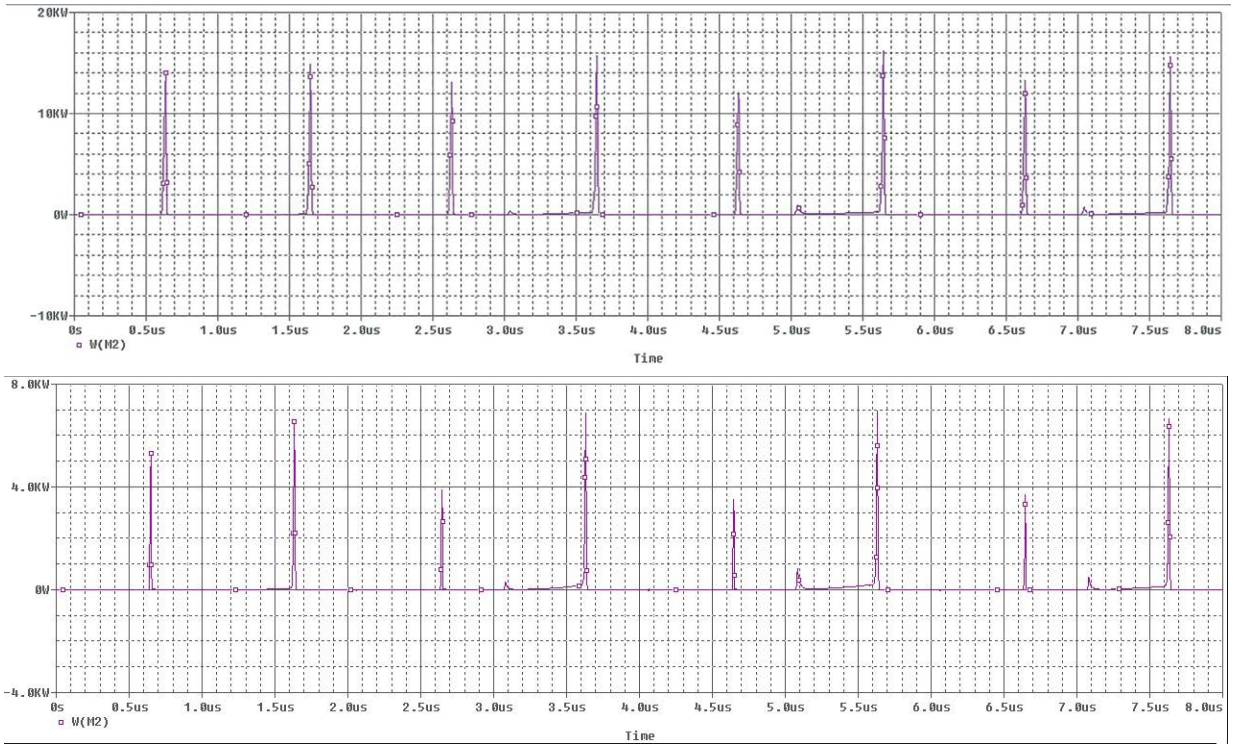

Figure 4. Simulated Waveforms. Top: Instantaneous Power on Q2 on non-ZVS topology, Bottom: Instantaneous power on Q2 with ZVS.

Source: Own Creation

Table 3. Instantaneous Power Characteristics of Power MOSFETs in the ZVS and Hard-Switched Converter at the time of gating

Value	ZVS				Non-ZVS			
Switching Device	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Instantanous Power at gating ZVS (kW)	7.6	4.8	2.7	7.7	14.5	14	16.1	15.6
Instantaneous Power at Turn-Off ZVS (kW)	14.5	7.3	7.7	6.7	20.3	14.8	19.4	16.8

Source: Own Creation

When the theoretical computed dead time was introduced in the switching scheme of the converter and compared against its hard-switched counterpart it was found that the commutation losses at turn-on are reduced to almost half. The instantaneous power waveform for switch $Q2$ when operating at ZVS and hard switching scheme is depicted in figure 4.

CONCLUSION

The Phase-Shifted PWM control can provide Zero-Voltage-Switching to the conventional Full-Bridge DC/DC converter. This mode of operation can bring important benefits such as high frequency operation without increased commutation losses. This particular advantage allows the size reduction in magnetic components such as transformers and filter inductors, however turn-off losses cannot be avoided in this switching scheme. The Phase-Shifted ZVS Full-Bridge converter makes a great choice for medium to high power applications, however the design process must be carried out carefully and the operation boundaries of the converter must be well defined to achieve an efficient ZVS operation, especially at low-load.

FINANCIAMIENTO

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